DAC Data(6) → 0
DAC Data(1) → DAC Sel(4)
DAC Data(2) → DAC Sel(1)
DAC Data(3) → DAC Sel(0)
Cl-Mode → Cl-Mode
DAC EN → DAC EN
(Vout) → 0
(Vref) → 0
+15V → +15V
-15V → -15V
+5V → +5V
Gnd → Gnd

DAC PCB

Front panel PCB

+SV → a
Gnd → a
DAC Sel(4) → a
DAC Sel(1) → a
DAC Sel(0) → a
FP Sel → a
FP Scale → a
FP Add S → a
FP Rst → a
FP BIP → a
Localsw → a
Listener → a
FP Force(3) → a
Vout → a
Abnd → a
Abnd → a

Front

ATN → 1
REN → 0
IFC → 0
NOAC → 0
NRFD → 0
DAV → 0
SRE → 0
Gnd → 0
Gnd → 0
EDT → 0
Data Listening → 0
Data LDM → 0

HP18 Connector PCB

HP18 PCB
93C14
4-bit Latch

9324
5-bit Comparator

74L03
Not as '93

96L02
Dual Monostable
Theory of DAC combination

DAC consists of 3 R-2R ladders, 1 for each decade.
Output impedance of each DAC = 50 kΩ. They are combined as shown on DAC PCB diagram sheet 2. So, representing each DAC as a voltage source in series with 50 kΩ, the combination is equivalent to:

\[ V = \frac{V_1}{250k} \times 50k + \frac{V_2}{50k} \times 50k + \frac{V_3}{50k} \times 50k \]

Least Significant Digit

Using the superposition principle:

For \( V_2 \):

\[ I_2 = \left( V_2, 0.00947 \right) \text{mA} \]

For \( V_1 \):

\[ I_1 = \left( V_1, 0.00947 \right) \text{mA} \]

For \( V_0 \):

\[ I_0 = \left( V_0, 0.00947 \right) \text{mA} \]

So \( I = I_0 + I_1 + I_2 = 0.000947 (V_0 + 10V_1 + 100V_2) \text{mA} \)

\[ V = 50I = 0.00474 \, (V_0 + 10V_1 + 100V_2) \]

\[ V_{\text{Ref}} = 10.36V \]

DAC set to 999 → DAC output (at pin3 of U1, say) = \( V_{\text{Ref}} \cdot 999 \cdot 0.00474 \leq 3.07V \)

At TP (4) \( -2.2 \times \text{DAC output} = 6.14V \)
At output \( \Rightarrow 2 \times 6.14 \times 161 \approx 9.9V \)